Curriculum of Sebastiano Fabio Schifano

ORCID	0000-0002-0132-9196
RESEARCHER ID	C-3555-2012
SCOPUS AU-ID	12782544700

Education, and positions

1994			Degree in Computer Science at University of Pisa.
Mar 1995	-	Mar 1997	Research associate at CNR "Istituto di Elaborazione dell'Informazione" (IEI).
Feb 1997	-	Oct 2006	Research associate at "Istituto Nazionale di Fisica Nucleare" (INFN).
Nov 2006	-	May 2019	Research associate (RU) at University of Ferrara, SSD INF/01.
Jun 2019	-	today	Associate Professor (PA) at University of Ferrara, SSD INF/01.

Research Activity

The research activities have mainly been focused on the design and exploitation of high performance computing systems for scientific applications of complex problems, like Lattice Gauge Theory (LQCD), fluid-dynamics simulations based on Lattice Boltzmann Methods and Monte Carlo simulations of Spin Glasses. During my period at INFN I had a major role in the development of the APEmille and apeNEXT projects. I have been deeply involved in the development of architecture of the processor and the network communication system. Within the framework of the APE projects I was responsable for the developmement of the "SHAKER", a software implementing the back-end steps of the compilation chain to optimize and scheduling the VLIW micro-instructions. I also partecipated in the development of the operating system. In 2005 I was co-autor of the proposal of the Janus system. Janus is a heterogeneous massively parallel system FPGA-based, developed by a collaboration of Spain and Italy. Janus has been developed mainly as spin-glass simulation engine, but it can be easily reconfigured for others applications. In the framework of this project I was responsable for the design of the architecture of the system, and I coordinated the development of the low-level interface between the boards and the host. In 2007 I was co-autor of the proposal for the QPACE project, a German project to develop a massively parallel system based on IBM Cell-BE processors, interconnected by a custom 3D-mesh. In the framework of the QPACE project I was in charge of designing and developing the logic of the network processor implemented on FPGA. My main research interests are in the field of parallel programming, code optimization, design of parallel systems and performance analysis of processors. I'm member of the reviewer panel of the International Journal of High Performance Computing Applications (IJHPCA, SAGE) and Parallel Computing Systems and Applications (PARCO, Elsevier) journal. I'm member of the Register of Expert Peer-Reviewers for Italian Scientific Evaluation (REPRISE).

Partecipation at National and International Projects

1. 01.01.2009 - 31.12.2011: INFN-Ferrara coordinator and task-leader of the EU-FP7 Hadron-Physics2 (HP2).
2. 01.01.2010 - 31.12.2014: local coordinator of the JANUS2 project funded by: EU-ERDF/2007-2013, FEDER project UNZA08-4E-020, EU-FP7/2007-2013, ERC grant agreement no.247328, MICINN (Spain), da Junta de Extremadura (contract GR101583).
3. 01.01.2012 - 31.12.2014: scientific coordinator of the *Computing on Knights Architectures* (COKA) project funded by INFN.
4. 01.01.2012 - 31.12.2014: INFN-Ferrara coordinator and task-leader of the EU-FP7 Hadron-Physics3 (HP3).
5. 01.01.2015 - 31.12.2018: INFN-Ferrara coordinator of the *Computing on SoC Architecures* (COSA) funded by INFN.
6. 01.09.2017 - 28.02.2021: INFN-Ferrara coordinator of the EU H2020 EuroEXA H2020-EU.1.2.2. - FET Proactive.
7. 01.06.2018 - 31.05.2022: member and WP-leader of WP5 *Training* of the EU Joint Doctorate (EJD) STIMULATE project.
8. 01.01.2016 - 14.10.2018: member and task coordinator of the EU Erasmus+ Capacity Building *Towards Open Resources Using Services* (TORUS).
9. 15.11.2018 - 14.11.2021: member and task coordinator EU Erasmus+ Capacity Building *Master On New Technologies Using Services: BigData/CloudComputing for Environmental Data* (MONTUS).
10. 01.01.2019-31.12.2021: PI of the project "Experimenting with Quantum Computing" (EQC) funded by INFN.
11. 01.01.2021 - 31.12.2021: PI of the project *Identificazione di una signature per la predizione della progressione della calcificazione della valvola aortica*, funded by Regione Emilia Romagna, Alte competenze per la ricerca e il trasferimento tecnologico finanziato dal "Programma Operativo Fondo Sociale Europeo" 2014/2020 (PO-FSE 2014/2020).

Presentations at peer-reviewed conferences (most recent)

1. *8th International Conference on Parallel Processing and Applied Mathematics* (PPAM), September 13-16 2009, Wroclaw, Poland. Title: *Monte Carlo Simulations of Spin Glass on the Cell Broadband Engine.*
2. *State of the Art in Scientific and Parallel Computing* (PARA), June 6-9 2010, Reykjavik, Iceland. Title: *Monte Carlo Simulations of Spin Systems on Multi-core Processors.*
3. *High Performance Computing Symposium* (HPC), April 3-6 2011, Boston, MA USA. Title: *Lattice Boltzmann Method Simulations on Massively Parallel Multi-core Architectures.*
4. *International Conference on Computational Science* (ICCS), June 1-3 2011, Singapore. Title: *Optimization of Multi-Phase Compressible Lattice Boltzmann Codes on Massively Parallel Multi-Core Systems.*
5. *9a International Conference on Parallel Processing and Applied Mathematics* (PPAM), September 11-14 2011, Torun, Poland. Title: *A multi-GPU implementation of a D2Q37 Lattice Boltzmann Code.*
6. *Innovative Parallel Computing 2012* (INPAR), May 13-14 2012, San Jose, CA USA. Title: *Implementation and Optimization of a Thermal Lattice Boltzmann Algorithm on a multi-GPU cluster.*
7. *24th International Conference on Parallel Computation Fluid Dynamics* (PARCFD), May 21-25 2012, Atlanta, GE USA. Title: *Performance Impact of AVX Instructions on a D2Q37 Lattice Boltzmann Scheme.*
8. *Conference on Computational Physics* (CCP), October 14-18 2012, Kobe, Japan. Title: *Exploiting parallelism in many-core architectures: a test case based on Lattice Boltzmann Models.*
9. *10th International Conference on Parallel Processing and Applied Mathematics* (PPAM), September 8-11 2013, Warsaw, Poland. Title: *An optimized Lattice Boltzmann code for BlueGene/Q.*
10. *20th International Conference on Computing in High Energy and Nuclear Physics* (CHEP), October 14-18 2013, Amsterdam, The Netherlands. Title: *Computing on knights and kepler architectures.*
11. *25th Int. Symp. on Computer Architecture and High Performance Computing* (SBAC-PAD), October 23-26 2013, Porto de Galinhas, Brazil. Title: *Benchmarking GPUs with a Parallel Lattice-Boltzmann Code.*
12. *International Conference on Computational Science* (ICCS), June 10-12 2014, Cairns, Australia. Title: *A portable OpenCL Lattice Boltzmann code for multi- And many-core processor architectures.*
13. *6th Conference on Computational Methods in Marine Engineering*, June 15-17, 2015, Rome, Italy. Title: *Using Accelerator to Speed-Up Scientific and Engineering Codes: Perspective and Problems.*
14. *International Conference on High Performance Computing and Simulation*, July 20-24 2015, Amsterdam, The Netherlands. Title: *Optimizing Communications in multi-GPU Lattice Boltzmann Simulations.*
15. *11th International Conference on Parallel Processing and Applied Mathematics*, September 6-9 2015, Krakow, Poland. Title: *Experience on vectorizing Lattice Boltzmann kernels for multi- and many-core architectures.*
16. *12th International Conference on Parallel Processing and Applied Mathematics*, September 10-13 2017, Lublin, Poland. Title: *Early experience on using Knights Landing processors for Lattice Boltzmann applications.*
17. *13th Int. Conference on Parallel Processing and Applied Mathematics*, September 8-11 2019, Bialystok (Poland) "Early performance assessment of the ThunderX2 processor for lattice based simulations".

Invited talks at conferences and workshops (most recent)

1. *10th ORAP Forum and 28th SPEEDUP Workshop*, 5-6 October 2000, CERN, Geneve, Swiss. Title: *European Tflops Project for Lattice Quantum Chromodynamics.*
2. *Third German Perl Workshop*, February 28 - March 2, 2001, Saint Augustin, Bonn, Germany. Title: *CAOS: The APEmille Operating System.*
3. *HPTC 2004 Conference*, September 19-22, 2004, Chateau de Maffliers, Paris, France. Title: *Computing for Lattice QCD: apeNEXT.*
4. *Scalperf workshop 2007*, September 2-6 2007, Bertinoro, Italy. Title: *Lattice QCD on Cell.*
5. *26th IFAE conference*, March 26-28, 2008, Bologna, Italy. Title: *Monte Carlo simulations in statistical physics: Janus.*
6. *Scalperf Workshop 2008*, September 7-12, 2008, Bertinoro, Italy. Title: *Trends in Computing for Theoretical Physics.*
7. *Young Investigators Symposium*, October 13-15, 2008, Oak Ridge National Laboratory, USA. Title: *Computing Systems for Theoretical Physics.*
8. *eQPACE Workshop*, February 9-10, 2009, JSC Juelich, Germany. Title: *Implementation of the QPACE Torus Network.*
9. *Scalperf Workshop 2009*, September 20-24, 2009, Bertinoro, Italy. Title: *The QPACE Project.*
10. *SuperB: Computing R&D Workshop 2011*, July 4-7, 2011, Ferrara, Italy. Title: *Physics Simulations on multi- and many-core architectures.*
11. *NVIDIA Application Lab Kick-off Workshop*, Sep. 19-20, 2012, Juelich, Germany. Title: *Implementation and Optimization of a D2Q37 Lattice Boltzmann.*

12. *X Seminar on Nuclear, Subnuclear and Applied Physics*, June 2-8, 2013, Alghero, Italy. Title: *Multi- and many-core computing for Physics applications.*
13. *PRACE Summer School Enabling Applications on Intel MIC based Parallel Architectures*, July 8-11, 2013, Casalecchio di Reno, Bologna, Italy. Title: *LBM on multi- and many-core architectures.*
14. *NVIDIA Application Lab Workshop*, July 8-9, 2013, Juelich, Germany. Title: *Benchmarking GPU architectures with Lattice Boltzmann simulations.*
15. *NVIDIA Application Lab Workshop*, June 10-12, 2014, Juelich, Germany. Title: *Portability, Performance and Scalability of LB Codes for Accelerator based Architectures.*
16. *PADC Opening Workshop*, October 12-13, 2015, Juelich, Germany. Title: *Early experience on running GPU-based Lattice Boltzmann simulations on POWER8 systems.*
17. *Introductory School on Parallel Programming and Parallel Architecture for High-Performance Computing*, October 10th, 2016, ICTP Trieste, Italy. Title: *Parallel Approaches To Lattice Boltzman Methods.*
18. Keynote speaker al workshop *HPCXXL Winter Workshop*, Frebuary 8, 2017, CINECA, Bologna (ITALIA). Title: *On usability of HPC systems.*
19. Keynote speaker alla conferenza *The Eight International Conference on Advanced Communications and Computation* (INFOCOMP18) July 22 - 26, 2018, Barcelona, (SPAIN). Titolo del lavoro presentato: *Challenges in Programming Modern Parallel Systems.*

Organizations of conferences and workshops (most recent)

1. Organizer and member of the program commitee of *Non Perturbative Problems and Computational Physics: The Next Five Years*, 27-28 November 2003, Ferrara (Italy).
2. Member of the program commitee of *ACM Conference on Computing Frontiers* 2008, May 5-7, 2008, Ischia (Italy).
3. Organizer and chair of the workshop *Future HPC systems: the Challenges of Power-Constrained Performance*, organized as part of the *ACM International Conference on Supercomputing* (ICS) June 25, 2012, San Servolo - Venezia (Italy).
4. Member of the program commitee of *ACM International Conference on Supercomputing* (ICS), June 25-29, 2012, San Servolo - Venezia (Italy).
5. Member of the program commitee of *International Workshop on Energy-aware high performance Heterogeneous Architectures and Accelerators* (WEHA 2015), organized as part of the *International Conference on High Performance Computing & Simulation (HPCS 2015)*, July 20-24, 2015, Amsterdam, The Netherlands.
6. Member of the program commitee of *6th International Workshop in Performance Modeling, Benchmarking and Simulation of High Performance Computer Systems* (PMBS15), organized as part of the *ACM/IEEE Supercomputing 2015* (SC15), Nov. 15, 2015, Austin, TX (USA).
7. Organizer and chair of the workshop *Computing on Low-Power Architectures* (COLA), February 25-26 2016, Ferrara, Italy.
8. Organizer of the workshop *Distributed Computing Architectures And Environmental Science Applications*, June 6-10 2016, Ferrara, Italy.
9. Organizer of the workshop *International Workshop on Energy-aware high performance Heterogeneous Architectures and Accelerators* (WEHA 2016), organized as part of the *The International Conference on High Performance Computing & Simulation* (HPCS 2016), July 18-22, 2016, Innsbruck, Austria.
10. Member of the program commitee of *7th International Workshop in Performance Modeling, Benchmarking and Simulation of High Performance Computer Systems* (PMBS16), organized as part of the *ACM/IEEE Supercomputing 2016* (SC16), Nov. 13, 2016, Salt Lake City, UT (USA).
11. Member of the program commitee of the workshop *International Workshop on OpenPOWER for HPC* (IWOPH'17), part of the ISC High Performance, 22 June, 2017 Frankfurt (GERMANY).
12. Member of the program commitee of the *The Seventh International Conference on Advanced Communications and Computation* (INFOCOMP17) June 25 - 29, 2017, Venezia (ITALY).
13. Member of the program commitee of the *ParCo 2017: Mini-Symposium on Energy Aware Scientific Computing on low power and heterogeneous architectures*, organized as part of the *International Conference on Parallel Computing* (ParCo 2017), September 12-15, 2017, Bologna, Italia.
14. Member of the program commitee of the *8th International Workshop in Performance Modeling, Benchmarking and Simulation of High Performance Computer Systems (PMBS17)*, organizzato come parte della conferenza *ACM/IEEE Supercomputing 2017* (SC17), Nov. 13, 2017, Denver, CO (USA).
15. Member of the program commitee of the *International Workshop on OpenPOWER for HPC* (IWOPH'18), organized as part of the *ISC High Performance*, 28 June, 2018 Frankfurt (GERMANY).
16. Member of the program commitee of the *The Eight International Conference on Advanced Communications and Computation* (INFOCOMP18) July 22 - 26, 2018, Barcelona, (SPAIN).

17. Member of the program commitee and chair of the session *Machine/Deep Learning* of the workshop *9th International Workshop in Performance Modeling, Benchmarking and Simulation of High Performance Computer Systems* (PMBS18), organized as part of the *ACM/IEEE Supercomputing 2018* (SC18), Nov. 12, 2018, Dallas, TX (USA).
18. Organizer and chair of the workshop *Energy-efficient Computing on Parallel Architectures* (ECO-PAR18), organized as part of the *The Eight International Conference on Advanced Communications and Computation* (INFOCOMP18) July 22 - 26, 2018, Barcelona, (SPAIN).

Participation at European Panel

1. Italian representative member (2006-2007) of the "HPC in Europe Taskforce" (HET).
2. The "High Performance Computing in Europe Taskforce" was formed by representatives of European countries interested in shaping the European High Performance Computing Infrastructure. The initiative was instrumental to the establishment of the PRACE research infrastructure.

Member of editorial board

1. Co-editor, together with S. Bassini, A. Hoisie, D. J. Kerbyson e D. Pleiter, proceedings of the workshop *Future HPC systems: the Challenges of Power-Constrained Performance*, organized as part of the *ACM International Conference on Supercomputing (ICS)* June 25, 2012, San Servolo - Venezia (Italy). ACM, New York, NY, USA, ISBN 978-1-4503-1453-4.
2. Co-editor, tohether with D. Cesini, of special issue *Energy Aware Scientific Computing on Low Power and Heterogeneous Architectures* on Journal of Low Power Electronics and Applications (ISSN 2079-9268).
3. Guest Editor dello special issue "Energy-Efficient Computing on Parallel Architectures" della rivista Computation (ISSN 2079-3197)
4. Membro dell'Editorial Board della rivista Scientific Programming - Hindawi

Scientific visits

1. Scientific visitor at *Juelich Supercomputing Center* (Juelich - Germay). Dal 01.07.2009 al 31.08.2009
2. Scientific visitor at *Deutsches Elektronen-Synchrotron* (DESY) sezione di Zeuthen-Berlino (Germany). Dal 01.07.2011 al 31.08.2011

Awards

1. November 2009 and June 2010 Best GREEN500 HPC system: the HPC system developed within the QPACE project has been awarded as the top entry of the GREEN500 list (www.green500.org).
2. Best Paper Award *On Portability, Performance and Scalability of a MPI OpenCL Lattice Boltzmann Code* presented at *7th Workshop on UnConventional High Performance Computing 2014* (UCHPC 2014) August 25/26, Porto, Portugal.
3. Best Paper Award *Energy-performance tradeoffs for HPC applications on low power processors* presented at *8th Workshop on UnConventional High Performance Computing 2015* (UCHPC 2015) August 25, Vienna, Austria.
4. Best Paper Award *Performance Optimization of D3Q19 Lattice Boltzmann Kernels on Intel KNL* presented at *INFOCOMP 2018, The Eighth International Conference on Advanced Communications and Computation* July 22-26, 2018, Barcelona, Spain.

Short Publication List (most relevant)

[1] E. Calore, A. Gabbana, S.F. Schifano, and R. Tripiccione. "Optimization of lattice Boltzmann simulations on heterogeneous computers". In: *The International Journal of High Performance Computing Applications* (2019), pp. 124–139. ISSN: 1094-3420. DOI: 10.1177/1094342017703771. IF(2017)=2.015.

[2] C. Bonati, E. Calore, M. D'Elia, M. Mesiti, F. Negro, F. Sanfilippo, S.F. Schifano, G. Silvi, and R. Tripiccione. "Portable multi-node LQCD Monte Carlo simulations using OpenACC". In: *International Journal of Modern Physics C* 29.1 (2018). ISSN: 0129-1831. DOI: 10.1142/S0129183118500109. IF(2017)=0.919.

[3] E. Calore, A. Gabbana, S.F. Schifano, and R. Tripiccione. "Design and optimizations of lattice Boltzmann methods for massively parallel GPU-based clusters". In: *Analysis and Applications of Lattice Boltzmann Simulations*. IGI Global, 2018, pp. 54–114. ISBN: 978-152254761-7;1522547606;978-152254760-0. DOI: 10.4018/978-1-5225-4760-0.ch003.

[4] E. Calore, A. Gabbana, S.F. Schifano, and R. Tripiccione. "Early experience on using Knights Landing processors for Lattice Boltzmann applications". In: *Parallel Processing and Applied Mathematics*. Vol. 1077. Lecture Notes in Computer Science. Springer International Publishing, 2018, pp. 1–12. ISBN: 978-3-319-78024-5. DOI: 10.1007/978-3-319-78024-5_45.

[5] E. Calore, A. Gabbana, S.F. Schifano, and R. Tripiccione. "Software and DVFS tuning for performance and energy-efficiency on intel KNL processors". In: *Journal of Low Power Electronics and Applications* 8.2 (2018). ISSN: 20799268. DOI: 10.3390/jlpea8020018. IF(2017)=1.182.

[6] C. Bonati, S. Coscetti, M. D'Elia, M. Mesiti, F. Negro, E. Calore, S.F. Schifano, G. Silvi, and R. Tripiccione. "Design and optimization of a portable LQCD Monte Carlo code using OpenACC". In: *International Journal of Modern Physics C* 28.5 (2017). ISSN: 0129-1831. DOI: 10.1142/S0129183117500632. IF(2017)=0.919.

[7] E. Calore, A. Gabbana, S.F. Schifano, and R. Tripiccione. "Evaluation of DVFS techniques on modern HPC processors and accelerators for energy-aware applications". In: *Concurrency and Computation: Practice and Experience* 29.12 (2017), pp. 1–19. ISSN: 1532-0634. DOI: 10.1002/cpe.4143. IF(2017)=1.114.

[8] E. Calore, A. Gabbana, J. Kraus, E. Pellegrini, S.F. Schifano, and R. Tripiccione. "Massively parallel lattice-Boltzmann codes on large GPU clusters". In: *Parallel Computing* 58 (2016), pp. 1–24. ISSN: 0167-8191. DOI: 10.1016/j.parco.2016.08.005. IF(2017)=0.938.

[9] E. Calore, A. Gabbana, J. Kraus, S.F. Schifano, and R. Tripiccione. "Performance and portability of accelerated lattice Boltzmann applications with OpenACC". In: *Concurrency and Computation: Practice and Experience* 28.12 (2016), pp. 3485–3502. ISSN: 1532-0634. DOI: 10.1002/cpe.3862. IF(2017)=1.114.

[10] L. Biferale, F. Mantovani, M. Pivanti, F. Pozzati, M. Sbragaglia, A. Scagliarini, S.F. Schifano, F. Toschi, and R. Tripiccione. "An optimized D2Q37 Lattice Boltzmann code on GP-GPUs". In: *Computers & Fluids* 80 (2013), pp. 55–62. ISSN: 0045-7930. DOI: 10.1016/j.compfluid.2012.06.003. IF(2017)=2.221.

[11] F. Mantovani, M. Pivanti, S.F. Schifano, and R. Tripiccione. "Performance issues on many-core processors: A D2Q37 Lattice Boltzmann scheme as a test-case". In: *Computers & Fluids* 88 (2013), pp. 743–752. ISSN: 0045-7930. DOI: 10.1016/j.compfluid.2013.05.014. IF(2017)=2.221.